IN THE SPECIFICATION:

Please amend the specification as follows.

[0006] United States Patent 4,862,245 to Pashby illustrates a "leads-over-chip" (LOC) configuration, wherein the inner lead ends of a standard dual-in-line package (DIP) lead frame configuration extend over and are secured to the active ~~upper~~ surface of the semiconductor device through a dielectric layer. The bond wire length is shortened by placing the inner lead ends in closer proximity to a central row of die bond pads, and the lead extensions purportedly enhance heat transfer from the semiconductor device. However, the Pashby LOC configuration, as disclosed, relates to mounting and bonding a single semiconductor device with the inner lead ends of the lead fingers to the surface of the semiconductor device.

[0037] As further illustrated, the lead frame 10″ of the present invention further includes a second plurality of lead fingers 18″ which extends substantially inwardly and is downset at portions 20″ thereon to have portions 22″ thereof lying in a horizontal plane which is substantially slightly lower than the inactive bottom surface of the semiconductor device 100″, the portions 22″ of the lead fingers 18″ extending to the ends 106″ of the semiconductor device ~~100'~~ 100″, and lead finger portions 24″ which extend under the semiconductor device 100″, which help support the semiconductor device 100″, and terminate at ends 26″ outside the semiconductor device 100″ substantially adjacent a longer peripheral side 104″ of the semiconductor device 100″.